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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,894	12/08/2003	Herman Kwong	57983.000155	9607

7590 11/03/2006

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,894	KWONG ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/728,894 filed 12/08/2003 and amendment filed 09/05/2006.

2. Claims 1-18 are pending in the Application. Claims 10-14 have been withdrawn from the consideration as non-elected claims in the previous office action mailed 06/05/2006.

3. Applicants' Remarks have been fully considered and are persuasive.

Claim 10-14, previously withdrawn from consideration as a result of a restriction requirement 03/03/2006, hereby rejoined and fully examined for patentability under 37 CFR 1.104.

Because claims 10-14 previously withdrawn from consideration under 37 CFR 1.142 have been rejoined, **the restriction requirement as set forth in the Office action mailed on 03/03/2006 is hereby withdrawn**. In view of the withdrawal of the restriction requirement as to the rejoined inventions, applicant(s) are advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application. Once the restriction requirement is withdrawn, the provisions of 35 U.S.C. 121 are no longer applicable. See *In re Ziegler*, 443 F.2d 1211, 1215, 170 USPQ 129, 131-32 (CCPA 1971). See also MPEP § 804.01.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kida et al. (US Patent 5,877,942).

With respect to claim 1 Kida et al. teaches a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers (within improved apparatus for forming circuit card assembly (CCA), wherein printed wiring boards (PWB) with FPGA's and other devices mounted (col. 2, ll.24-25), and wherein PWB having multiple layers of interconnection paths (col. 2, ll.60-62)), the method comprising: assigning a set of one or more contacts of the PLD to one or more respective contacts of the electronic component based at least in part on a pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device, the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal routing device (within FPGA's, which are used for emulating ASIC (col. 1, ll.41-42; ll.57-60) including fabrication of the PWB to provide appropriate interconnection paths for interconnecting input/output pins of the FPGA's to each other or to external input/output devices (col. 1, ll.61-64), wherein PWB having multiple layers of interconnection paths

(col. 2, ll.60-62)); and wherein a set of interconnection paths are formed of terminal areas, traces and vias (col. 4, ll.52-53).

With respect to claim 10 Kida et al. teaches a method for mapping contacts of a programmable logic device (PLD) to contacts of an electronic component in a signal routing device having one or more layers (within improved apparatus for forming circuit card assembly (CCA), wherein printed wiring boards (PWB) with FPGA's and other devices mounted (col. 2, ll.24-25), and wherein PWB having multiple layers of interconnection paths (col. 2, ll.60-62)), the method comprising: determining a first pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device (within FPGA's, which are used for emulating ASIC (col. 1, ll.41-42; ll.57-60) including, and wherein a set of interconnection paths are formed of terminal areas, traces and vias (col. 4, ll.52-53)); determining a first contact assignment pattern for one or more contacts for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces (within severable traces and with all interconnection paths to or from terminal areas for use with user programmable input-output pins of the FPGA routed through at least one pair of vias (col. 4, ll.54-60); refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second pattern of electrically conductive traces routed from the respective contacts of the electronic component via one or more layers of the signal routing device (within re-working the interconnection paths of the PWB (col. 5, ll.23-34)); and determining a second contact assignment pattern for one or

more contacts of the PLD based at least in part on the second pattern of electrically conductive traces (col. 5, ll.35-43)); and wherein a set of interconnection paths are formed of terminal areas, traces and vias (col. 4, ll.52-53).

With respect to claim 15 Kida et al. teaches a signal routing device having one or more layers (within circuit card assembly (CCA), wherein PWB is mounted with FPGA and other devices (col. 2, ll.23-24) and PWB having multiple internal layers of interconnection paths (col. 2, ll.60-62)), and further comprising an electronic component having a plurality of contacts (within emulated ASIC or other devices having plurality of input-output pins (col. 1, ll.61-63)); a programmable logic device (PLD) having a plurality of contacts (within FPGA having plurality of input-output pins (col. 1, ll.62-63); and a plurality of electrically conductive traces connecting contacts of the PLD to respective contacts of the electronic component, the plurality of electrically conductive traces routed from the respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device (within FPGA's, which are used for emulating ASIC (col. 1, ll.41-42; ll.57-60) including fabrication of the PWB to provide appropriate interconnection paths for interconnecting input/output pins of the FPGA's to each other or to external input/output devices (col. 1, ll.61-64), wherein PWB having multiple layers of interconnection paths (col. 2, ll.60-62); wherein the one or more contacts of the PLD are assigned based at least in part on a pattern formed by the electrically conductive traces routed from the respective contacts of the electronic component via the one or more channels, wherein the one or more channels being formed by arranging vias for contacts of at least the electronic component in the signal

routing device (within a set of interconnection paths are formed of terminal areas, traces and vias (col. 4, ll.52-53)).

With respect to claims 2-9, 11-14 and 16-18 Taylor teaches:

Claim 2: further comprising the step of forming electrically conductive traces between the set of one or more contacts of the PLD and the respective contacts of the electronic component accordance with the pattern of electrically conductive traces (col. 5, ll.52-59);

Claim 3: wherein one or more of the electrically conductive traces are routed to respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device (within fabrication of the PWB to provide appropriate interconnection paths for interconnecting input/output pins of the FPGA's to each other or to external input/output devices (col. 1, ll.61-64), wherein PWB having multiple layers of interconnection paths (col. 2, ll.60-62));

Claim 4: further comprising the steps determining first pattern of electrically conductive traces routed from respective contacts of the electronic component via at least one channel of the one or more channels (within FPGA's, which are used for emulating ASIC (col. 1, ll.41-42; ll.57-60) including, and wherein a set of interconnection paths are formed of terminal areas, traces and vias (col. 4, ll.52-53)); determining a contact assignment pattern for one or more contacts of the PLD based at least in part on the first pattern of electrically conductive traces (within severable traces and with all interconnection paths to or from terminal areas for use with user programmable input-output pins of the FPGA routed through at least one pair of vias (col. 4, ll.54-60)); and

refining the first pattern of electrically conductive traces based at least in part on the first contact assignment pattern to generate a second of electrically connective traces routed from the respective contacts of the electronic component via at least one of the one or more channels (within re-working the interconnection paths of the PWB (col. 5, ll.23-34));

Claim 5: wherein the one or more contacts of the PLD are assigned to the one or more respective contacts of the electronic component based at least in part on the second pattern of electrically conductive traces (col. 6, ll.38-45);

Claim 6: further comprising the step of: assigning one or more contacts of the PLD to one or more respective contacts of a second electronic component of the signal routing device based at least in part on a pattern of electrically conductive traces routed from respective contacts of the second electronic component via one or more channels formed at one or more layers of the signal routing device (col. 6, ll.41-48);

Claim 7: further comprising the step of: assigning one or more contacts of a second PLD to one or more respective contacts of the electronic component based at least in part on a second pattern of electrically conductive traces routed from respective contacts of the electronic component via one or more channels formed at one or more layers of the signal routing device (col. 8, ll.58-64);

Claims 8 and 16: wherein the one or more contacts of the PLD are assigned to the respective contacts of the electronic component by programming the PLD (col. 6, ll.41-45);

Claims 9, 11, 14 and 17: wherein the electronic component includes one of a group consisting of: a programmable logic device (PLD) and an application specific integrated circuit (ASIC) (col. 1, ll.57-60);

Claims 12, 13 as similar limitations of the claims 4 and 5 respectively, including creating contact assignment patterns according to a design change in the FPGA correcponding to the changes in the ASIC design (col. 8, ll.60-65);

Claim 18: wherein the electrically connective traces are routed to the respective contacts of the PLD via one or more channels formed at one or more layers of the signal routing device (within fabrication of the PWB to provide appropriate interconnection paths for interconnecting input/output pins of the FPGA's to each other or to external input/output devices (col. 1, ll.61-64), wherein PWB having multiple layers of interconnection paths (col. 2, ll.60-62)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

VUTHE SIEK
PRIMARY EXAMINER
For Whitmore